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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,005	02/25/2004	Shigeru Fujita	SON-2612/DIV	9742

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EXAMINER

LE, THAO X

ART UNIT PAPER NUMBER

2814

DATE MAILED: 05/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

8/1

Office Action Summary	Application No. 10/785,005	Applicant(s) FUJITA, SHIGERU	
	Examiner Thao X. Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 April 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 4, 13 and 15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4, 13 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 1, 4, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US6383873 to Hegde et al.

Regarding claim 1, Hegde discloses a semiconductor device fig. 4 comprising: a semiconductor substrate 102, col. 2 line 16, a high dielectric-constant film 106 on the semiconductor substrate 102, wherein the high-dielectric constant film 106 is composed of Al₂O₃, col. 2 line 50, having a thickness of approximately 2.5nm, col. 2 line 63, and a nitride layer 108, col. 3 lines 20-22, on the high-dielectric-constant film 106, fig. 4, the nitride layer 108 has a thickness of about less than 0.9 nm, col. 3 line 58, a gate electrode 110 comprising a p-type impurity-contained layer, col. 4 line 48, on the nitride layer 108, fig. 4, wherein the p-type impurity layer 110 is a boron-contained silicon layer, col. 4 lines 47-48, and a lightly doped drain (LDD) structure 126, fig. 4, a formation of a side wall 128, fig. 4, adjacent to the gate electrode 110, and a second introduction of boron (p-type dopant) to the substrate to form source and drain regions 124, fig. 4.

But, Hedge does not disclose introduction of boron into the substrate to form a LDD structure, and a second introduction of boron (p-type dopant) to the substrate to form source and drain regions.

However, Hedge discloses the gate 100 can be doped with boron (P-type dopant) or phosphorous (N-type dopant) to create a P-type or N-type gate that would imply a gate electrode for either NMOS or PMOS having N-type or P-type S/D and LLD regions, respectively. Thus, it is obvious that Hedge's disclosure would include or can be used to make a PMOS having P-type LLD and P-type S/D or NMOS having a N-type LLD and N-type S/D. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Hedge as claimed because such structure is well established in the art, see Sun (2003/0141560) in fig. 8, Gardner (6531364) fig. 13, col. 1 lines 25-35, or Gardner (6429052) fig. 8 in col. 5 lines 55-57 and col. 6 line 10-15.

The process limitations "introducing nitrogen into a top surface portion of the high-dielectric-constant film, wherein introducing nitrogen into the top surface portion comprises introducing nitrogen gas at 300-400 sccm for approximately 20-60 seconds at approximately 10-100 mTorr" in claim 1, do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Regarding claims 4 and 15, Hedge discloses the semiconductor device wherein the semiconductor substrate 102 is a silicon substrate or a silicon layer, col. 2 line 18.

Regarding claim 13, Hedge discloses a semiconductor device fig. 4 comprising: a semiconductor substrate 102, col. 2 line 16, a gate insulating film 106 on the

semiconductor substrate 102, and a gate electrode 110 formed on the gate insulating film 106 and including a P-type impurity-contained layer (boron doped), col. 4 line 48, wherein the p-type impurity layer is a boron-contained silicon layer; wherein the gate insulating film 106 includes a high dielectric-constant film 106 and a nitride layer 108 on the high-dielectric constant film 106, wherein the high-dielectric constant film 106 is composed of Al_2O_3 , col. 2 line 50, having a thickness of approximately 2.5nm, col. 2 line 63, and a nitride layer 108, col. 3 lines 20-22, on the high-dielectric-constant film 106, fig. 4, the nitride layer 108 has a thickness of about less than 0.9 nm, col. 3 line 58, a lightly doped drain (LDD) structure 126, fig. 4, a formation of a side wall 128, fig. 4, adjacent to the gate electrode 110, a source and drain (S/D) regions 124, fig. 4.

But, Hedge does not disclose introduction of boron into the substrate to form a LDD structure, and a second introduction of boron (p-type dopant) to the substrate to form source and drain regions.

However, Hedge discloses the gate 100 can be doped with boron (P-type dopant) or phosphorous (N-type dopant) to create a P-type or N-type gate that would imply a gate electrode for either NMOS or PMOS having N-type or P-type S/D and LLD regions, respectively. Thus, it is obvious that Hedge's disclosure would include or can be used to make a PMOS having P-type LLD and P-type S/D or NMOS having a N-type LLD and N-type S/D. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Hedge as claimed because such structure is well established in the

art, see Sun (2003/0141560) in fig. 8, Gardner (6531364) fig. 13, col. 1 lines 25-35, or Gardner (6429052) fig. 8 in col. 5 lines 55-57 and col. 6 line 10-15.

The process limitations "introducing nitrogen into a top surface portion of the high-dielectric-constant film, wherein introducing nitrogen into the top surface portion comprises introducing nitrogen gas at 300-400 sccm for approximately 20-60 seconds at approximately 10-100 mTorr" in claim 1, do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Response to Arguments

3. Applicant's arguments with respect to claims 1 and 13 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

5. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thao X. Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M. Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to be 'Thao X. Le', with a long horizontal line extending to the right.

Thao X. Le
17 May 2006